REMARKS

Applicant notes with appreciation that, in the Office Action of October 31, 2006, claims 3, 4, 10 and 11 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, claims 1 and 6-8 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Application No. US 2002/0180685 A1 (hereinafter "Itakura et al.") in view of "A 12-Transistor PFM Demodulator for Analog Neural Networks Communication" (hereinafter "Mortara et al."). In addition, claims 2, 9 and 12-20 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable in view of Itakura et al., Mortara et al. and/or U.S. Patent Application No. 2004/0036670 A1 (hereinafter "Chung"). Furthermore, claim 15 was rejected under 35 U.S.C. §112, second paragraph, because the term "said second output" on line 12 is considered indefinite. Similarly, claim 16 was rejected under 35 U.S.C. §112, second paragraph, because the claimed term "output node" is considered indefinite

In response, Applicant has amended claim 15 by replacing the term "said second output" on line 12 with the term "said second output transistor" to overcome the section 112 rejection. Applicant has also amended claim 16 by inserting the phrase "connected to said output transistor" after "output node" to overcome the section 112 rejection. In addition, Applicant has amended the independent claim 1 to include the subject matter of the dependent claim 2 and to delete the subject matter of the original dependent claim 5. Consequently, the dependent claim 2 was canceled. As a result, claim 3 was amended to maintain proper dependency. Applicant has also added a new claim 21, which recites the subject matter of the original dependent claim 5. As amended, Applicant respectfully asserts that the independent claim 1 is not obvious in view of the cited references, as explained below. Applicant also respectfully asserts that the independent claims 9 and 16 are not obvious in view of the cited references. In view of the following remarks, Applicant respectfully requests that the independent claims 1, 9 and 16, as well as the dependent claims 3, 4, 6-8, 10-15 and 17-21, be allowed.

I. Patentability of Independent Claims 1 and 9

As amended, the independent claim 1 includes the subject matter of the dependent claim 2. In the latest Office Action, the dependent claim 2 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable in view of Itakura et al., Mortara et al. and Chung. Similarly, the independent claim 9 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable in view of Itakura et al. and Chung. However, a *prima facie* case of obviousness for the independent claims 1 and 9 cannot be established because the cited references of Itakura et al., Mortara et al. and Chung even when combined do not teach or suggest all the limitations of the independent claims 1 and 9. In particular, the cited references even when combined do not teach or suggest the limitation of "*a memory operatively connected to said control terminal of said output transistor, said memory being configured to store a signal on said control terminal of said output transistor from a previous operating cycle in which said output transistor was activated,*" as recited in the amended independent claim 1, and the limitation of "a *memory connected to said control terminal of said output transistor, said memory being configured to store a signal on said control terminal from a previous operating cycle in which said output transistor was activated,*" as recited in the independent claim 9. Thus, Applicant respectfully asserts that the independent claims 1 and 9 are not obvious in view of the cited references of Itakura et al. Mortara et al. and Chung, and requests that these independent claims be allowed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

With respect to the dependent claim 2, the Office Action correctly states on page 11 that neither Itakura et al. nor Mortara et al. teaches "a memory operatively connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated." However, the Office Action then alleges on page 11 that the cited reference of Chung teaches "a memory (*See figure 11, element 530*) operatively connected to the control terminal of the output transistor (*See figure 11, element 510: driver amplifier; See figure 14: driver amplifier, element 512; driving stage*)" that is "configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated (*[0078]; [0080]; [0081]*). Applicant respectfully disagrees with this analysis.

The previous data latch (530) in Fig. 11 of Chung is described in paragraph [0080] as a component that "latches 2 bits of 6 bits of the display data DD and outputs previous data (PD<5><4>) of 2 bits in response to a previous data latch signal BC_CLK." As shown in Fig. 6 and described in paragraphs [0054] and [0056] of Chung, the previous data is display data DD from the display data latch (310). Clearly, the previous data latch (530) does not store any signal on a control terminal of an output transistor. Therefore, the cited references of Itakura et al., Mortara et al. and Chung even when combined do not disclose the limitation of "*a memory operatively connected to said control terminal of said output transistor, said memory being configured to store a signal on said control terminal of said output transistor from a previous operating cycle in which said output transistor was activated,*" as recited in the amended independent claim 1. As such, Applicant respectfully requests that the independent claim 1 be allowed.

The above remarks are also applicable to the independent claim 9, which includes a similar limitation. As such, Applicant respectfully requests that the independent claim 9 be allowed as well.

II. Patentability of Amended Independent Claim 16

The independent claim 16 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable in view of Itakura et al. and Chung. However, a *prima facie* case of obviousness for the independent claim 16, which is now amended, cannot be established because the cited references of Itakura et al. and Chung even when combined do not teach or suggest all the limitations of the independent claim 16. In particular, the cited references even when combined do not teach or suggest the limitation of "*applying a stored signal to an output transistor in response to said input signal to produce an output signal on an output node connected to said output transistor,*" as recited in the independent claim 16. Thus, Applicant respectfully asserts that the independent claim 16 is not obvious in view of the cited references of Itakura et al. and Chung, and requests that this independent claim be allowed.

The Office Action correctly states on page 7 that the cited reference of Itakura et al. "does not mention applying a stored signal to an output transistor in response to the input signal to produce an output signal on the output node of the output transistor." However, the Office Action then asserts on page 7 that "Chung teaches a memory (*See figure 11, element 530*) connected to a control terminal of an output transistor (*See figure 11, element 510: driver amplifier; See figure 14: driver amplifier, element 512: driving stage*), applying a stored signal to an output transistor in response to an input signal to produce an output signal on the output node of the output transistor (*[0078]; [0080]; [0081]*)." Applicant respectfully disagrees with this analysis.

The previous data latch (530) in Fig. 11 of Chung is described in paragraph [0080] as a component that "latches 2 bits of 6 bits of the display data DD and outputs previous data (PD<5><4>) of 2 bits in response to a previous data latch signal BC_CLK." As described in paragraph [0081] of Chung, "[t]he bias control voltage generator 520 receives 2 bits of the display data DD as current data (CD<5><4>) of 2 bits, compares the current data (CD<5><4>) with the previous data (PD<5><4>), and generates the control signal VC." Thus, the bias control voltage generator (520) receives the previous data (PD<5><4>) of 2 bits from the previous data latch (530) and generates the control signal VC, which is composed of 2 bits of a high bit HSL

and a low bit LSL, as described in paragraph [0081]. As shown in Fig. 14 and described in paragraph [0087], the control signal VC from the bias control voltage generator (520) is used to control a switch (SW) in the driver amplifier (510). Thus, as disclosed in Chung, the stored signal in the previous data latch (530) is not applied to any output transistor. Therefore, the cited references of Itakura et al. and Chung even when combined do not disclose the limitation of "*applying a stored signal to an output transistor in response to said input signal to produce an output signal on an output node connected to said output transistor,*" as recited in the amended independent claim 16. As such, Applicant respectfully requests that the amended independent claim 16 be allowed.

II. Patentability of Dependent Claims 3, 4, 6-15, 17-21

Each of the dependent claims 3, 4, 6-15, 17-21 depends on one of the independent claims 1, 9 and 16. As such, these dependent claims include all the limitations of their respective base claims. Therefore, Applicant submits that these dependent claims are allowable for at least the same reasons as their respective base claims.

Applicant respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
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